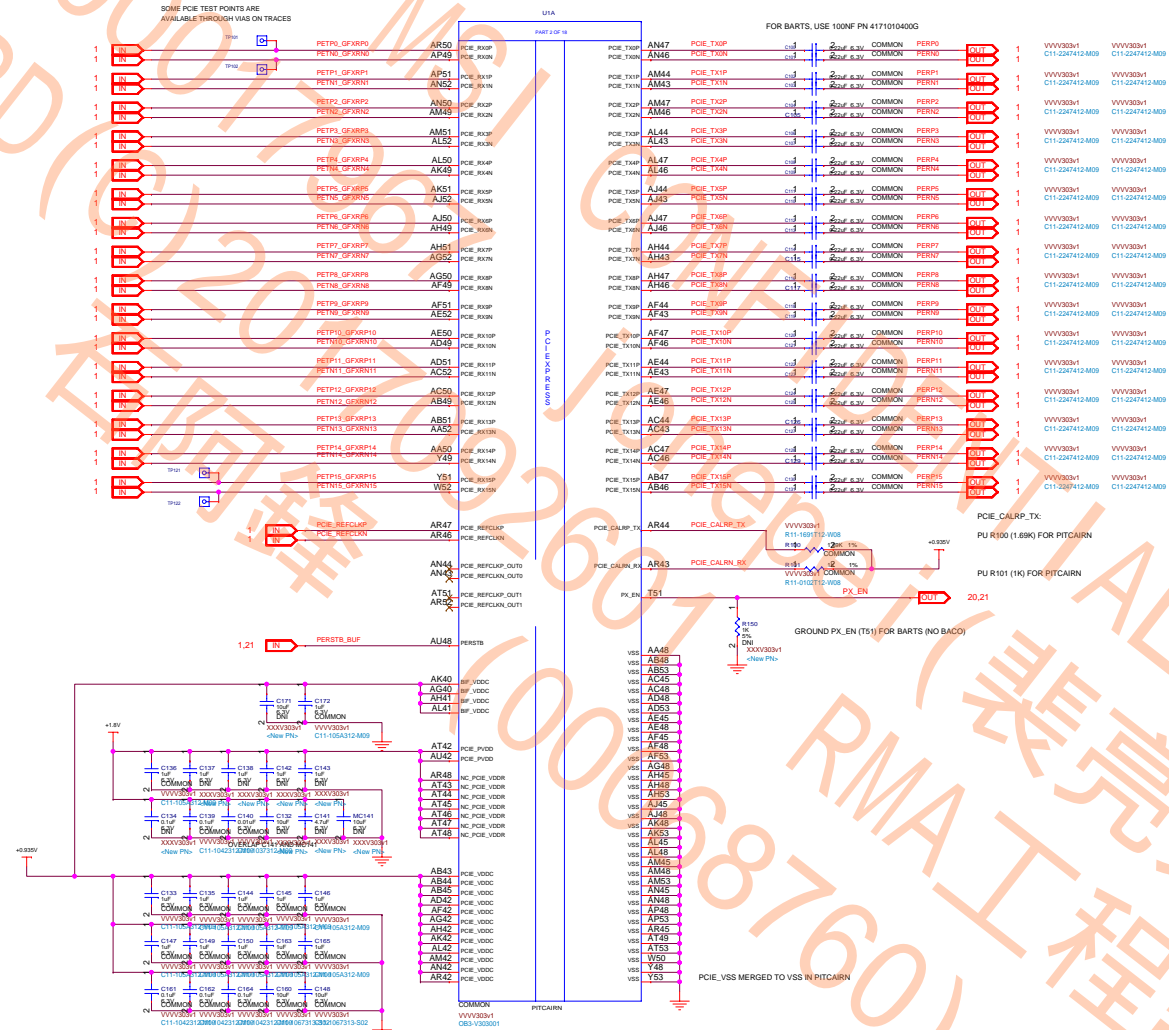
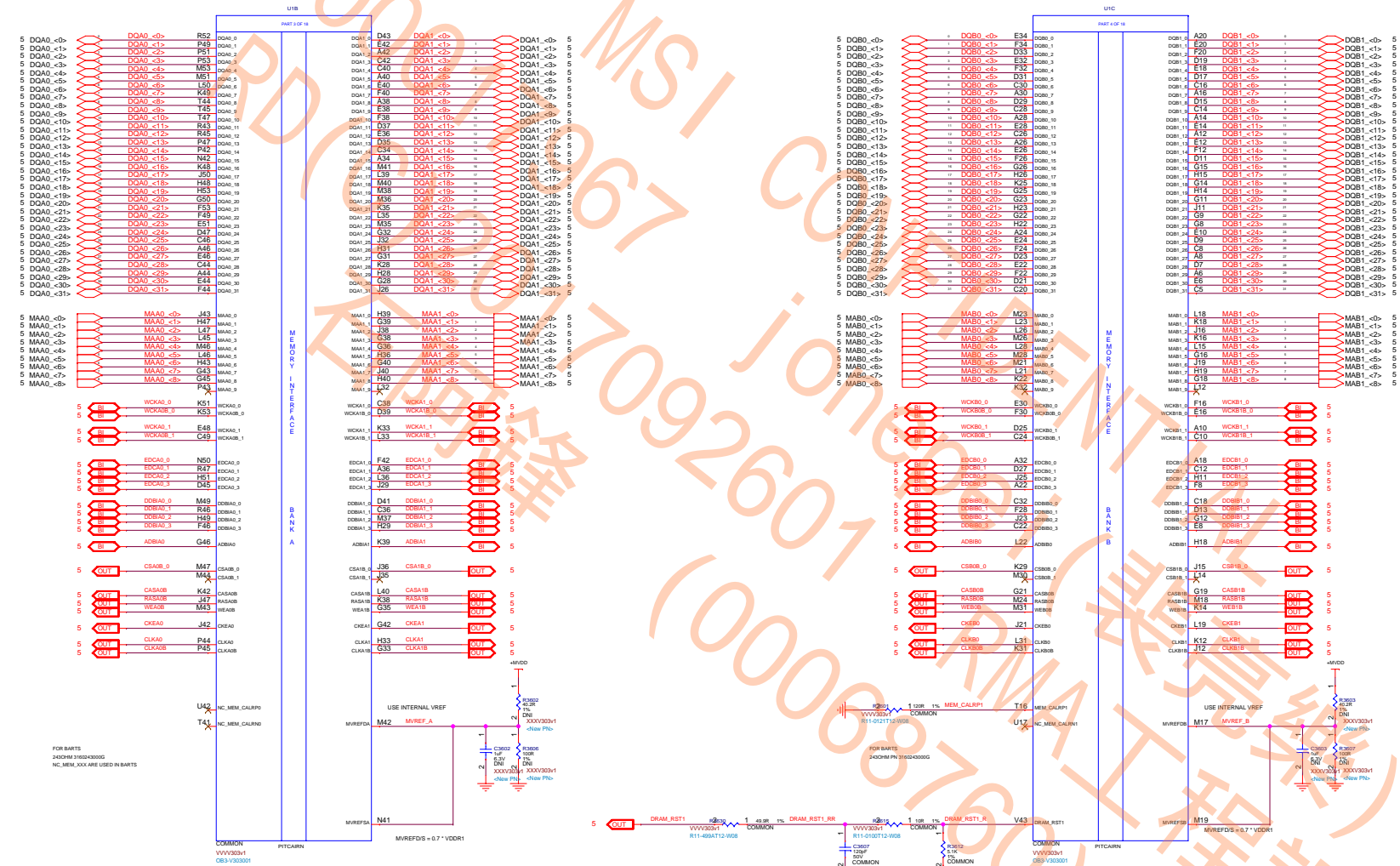


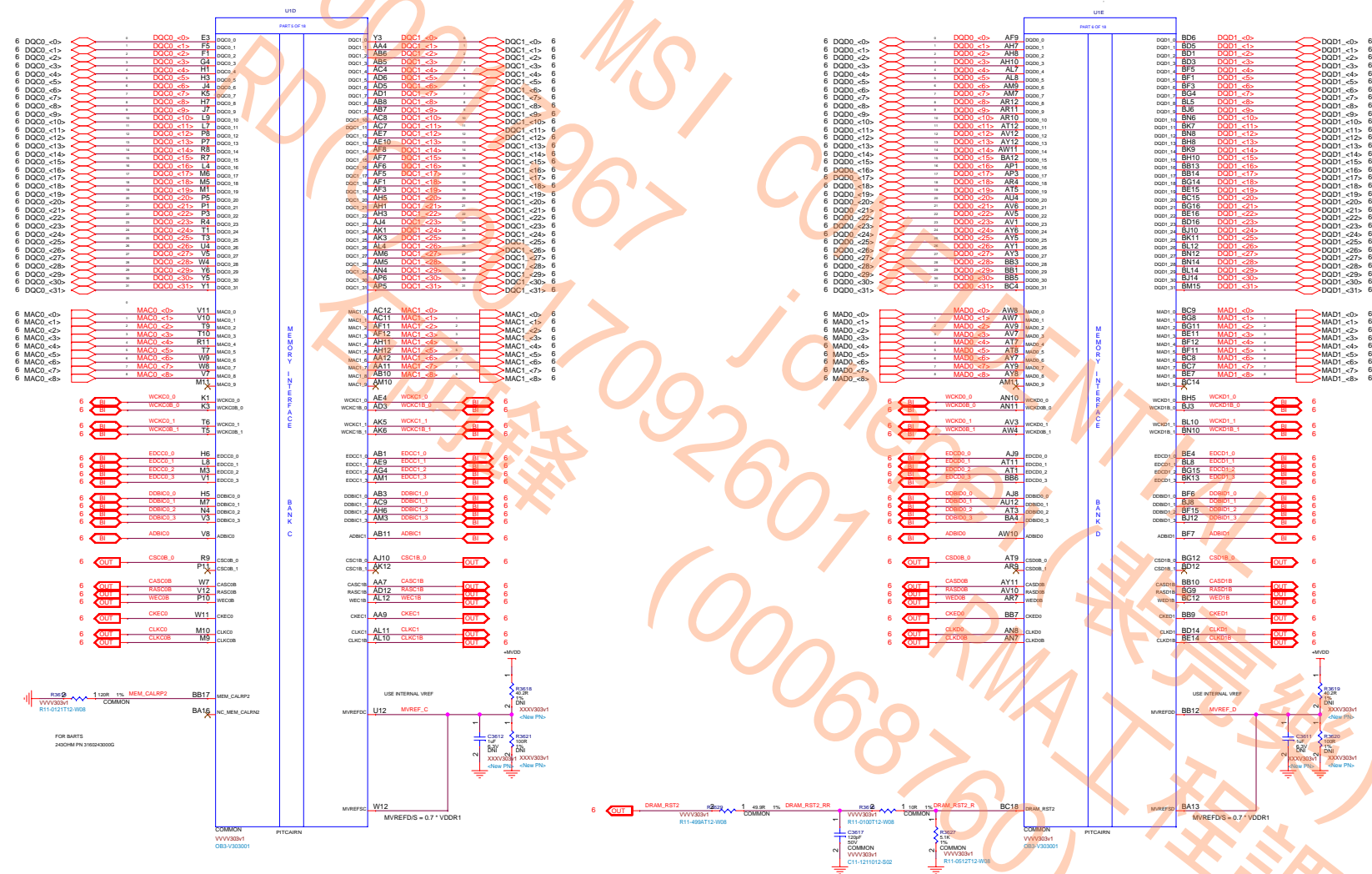
(2) CURACAO PCIE INTERFACE



(3) CURACAO MEM INTERFACE CH AB



(4) CURACAO MEM INTERFACE CH CD

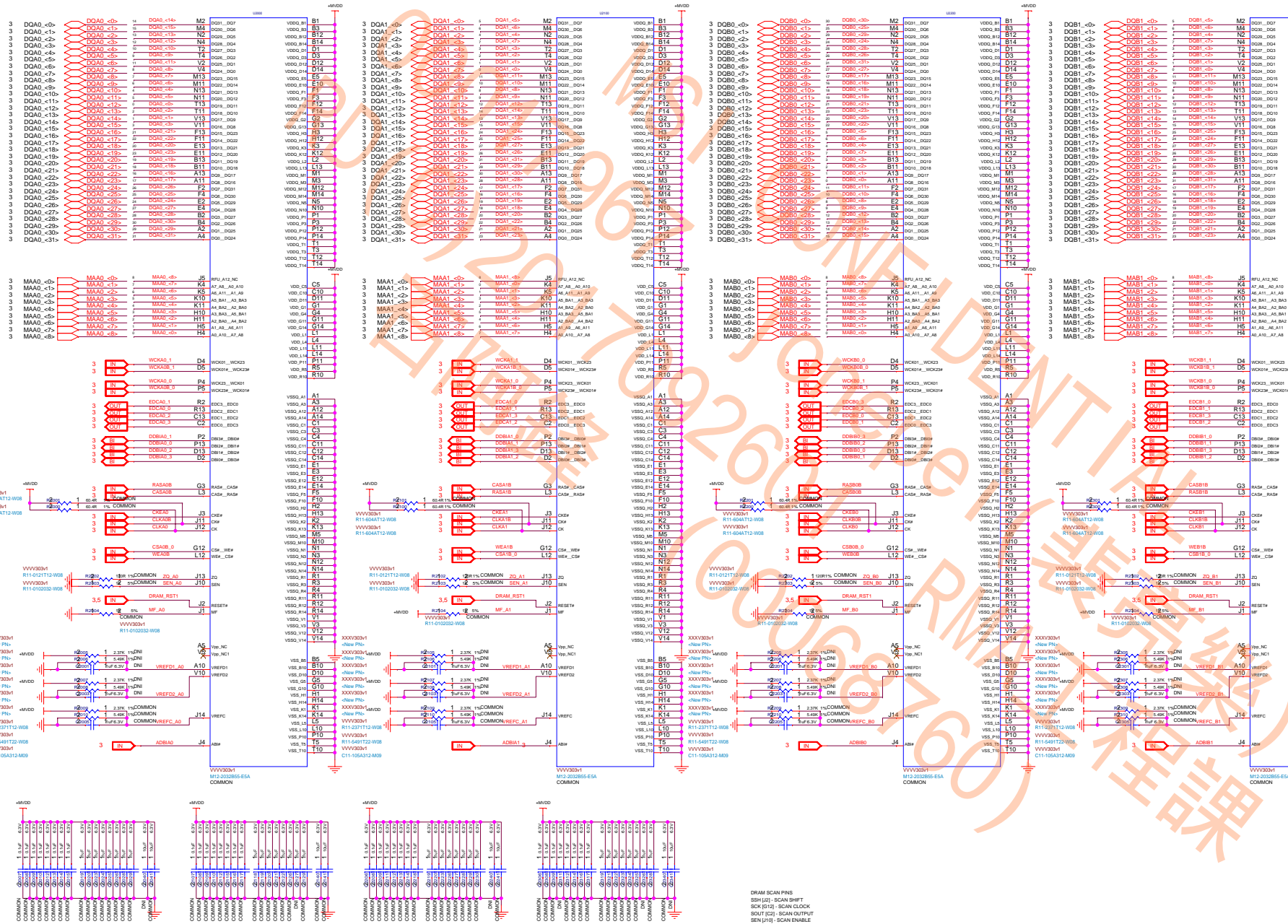


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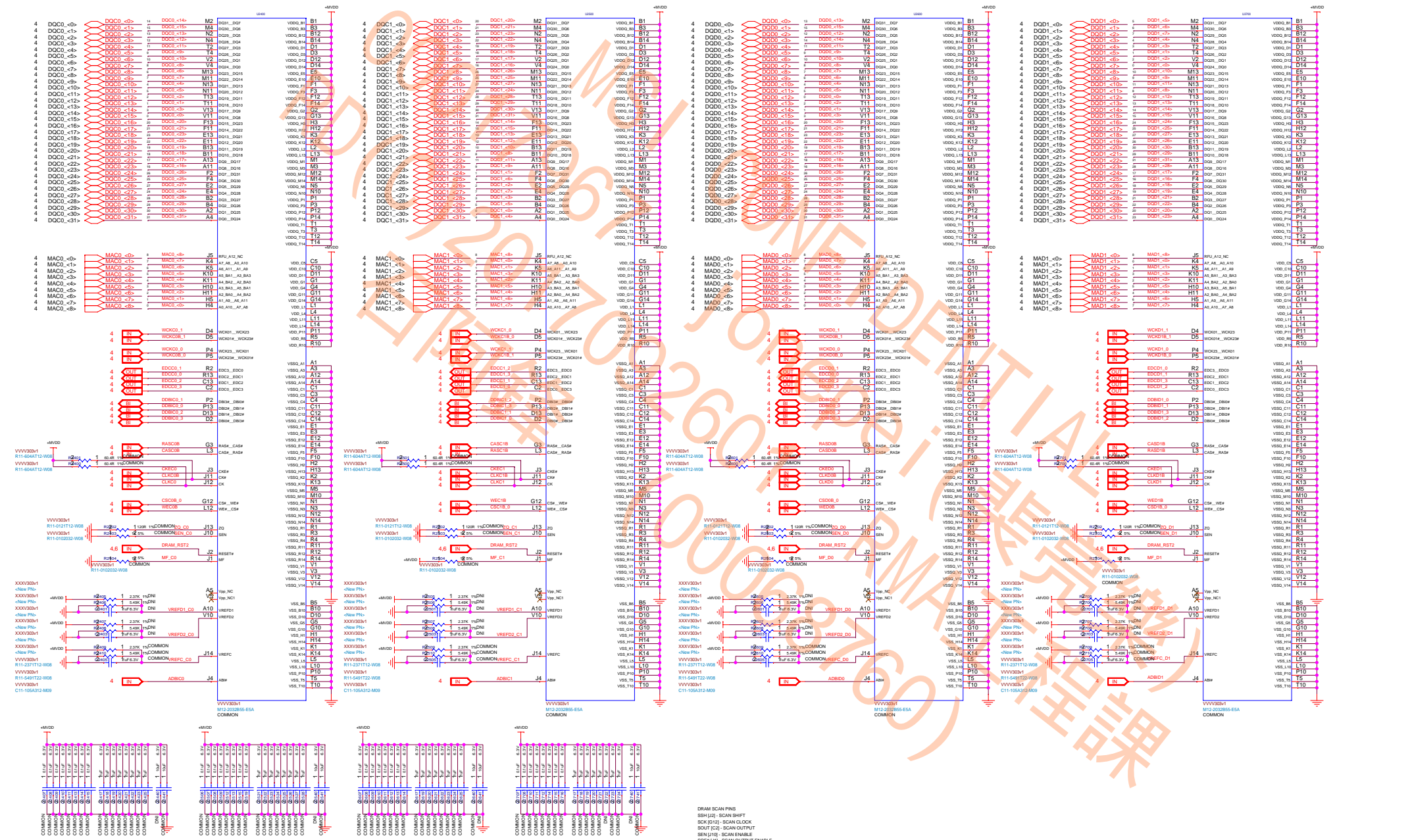
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Size Custom	Document Description 04 CURACAO PITCAIRN MEM CH CD	Rev 1.0
Date: Thursday, August 01, 2013		Sheet 4 of 24

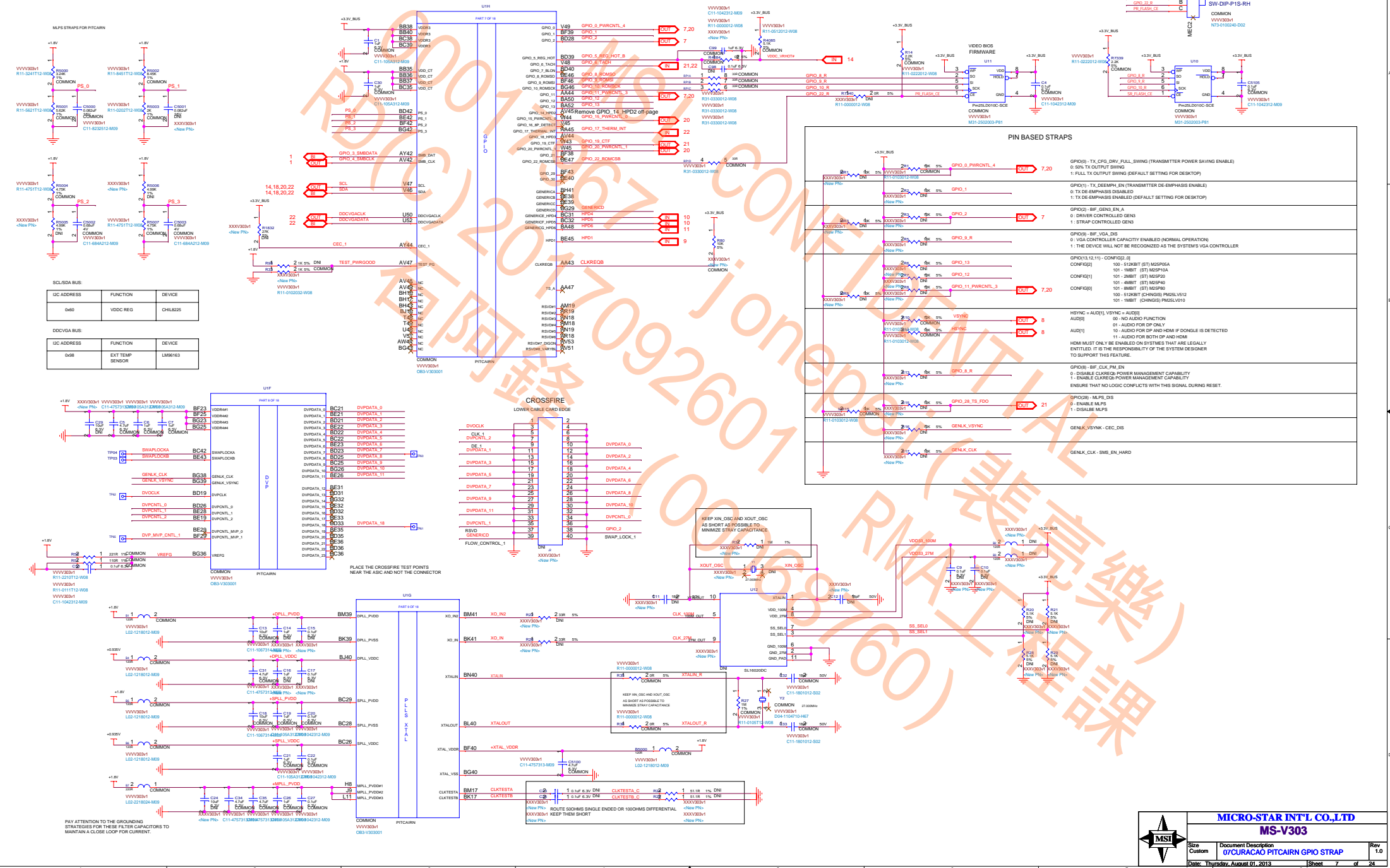
(5) GDDR5 MEM CH AB

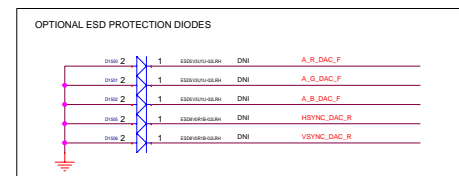


(6) GDDR5 MEM CH CD

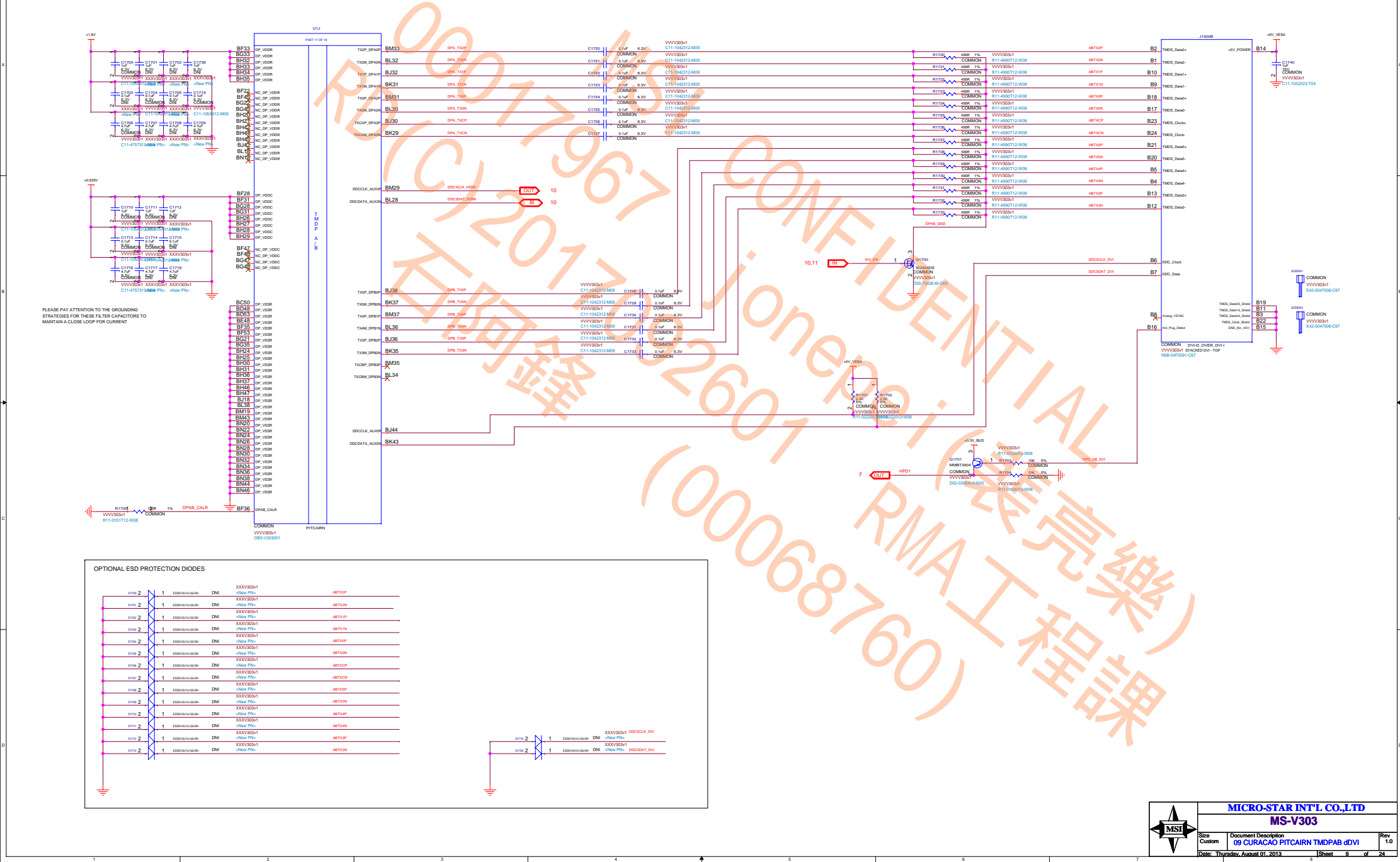


(7) CURACAO GPIO STRAP CF PLL XTAL

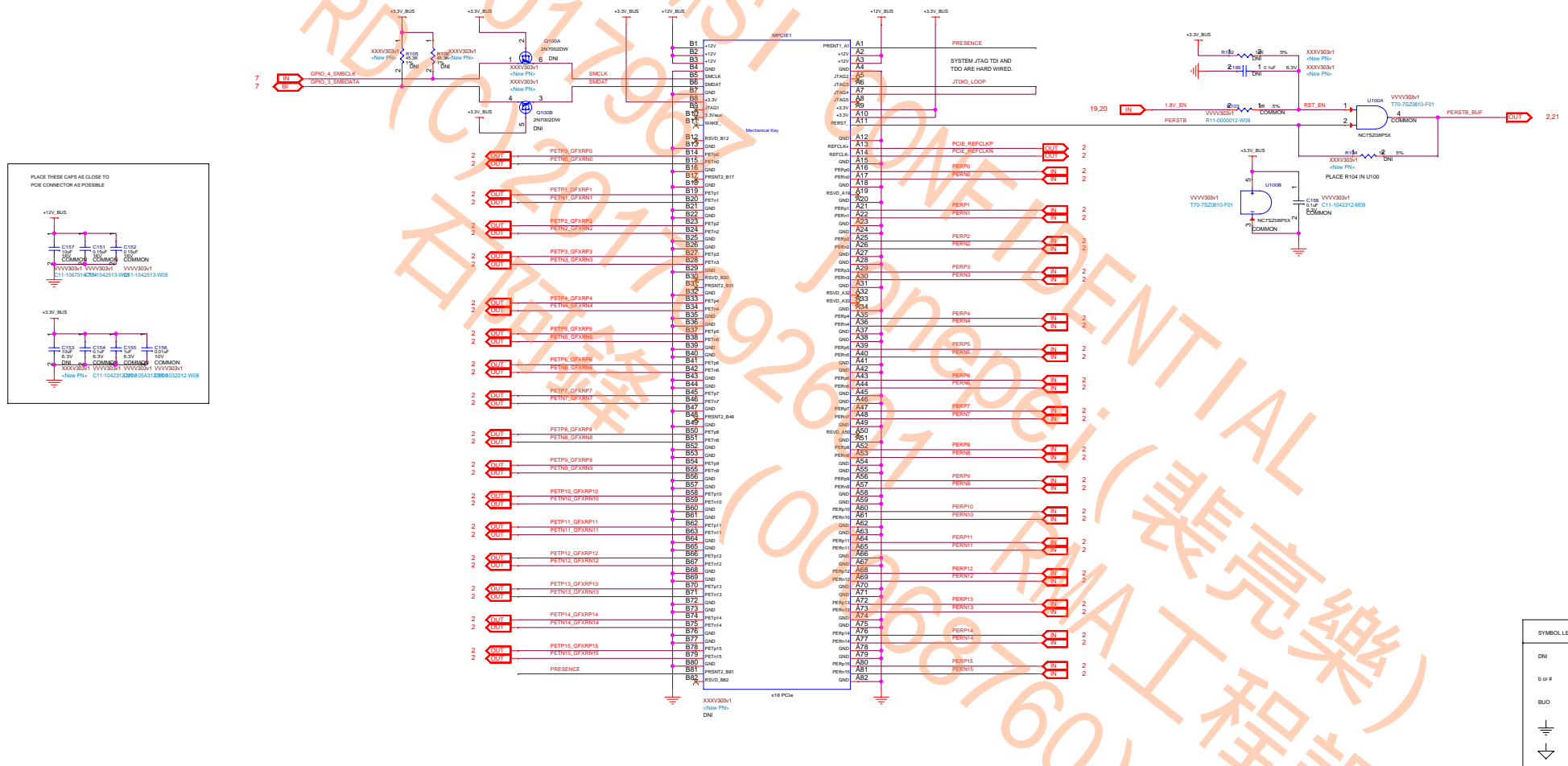






(9) CURACAO TMDPAB sDVI

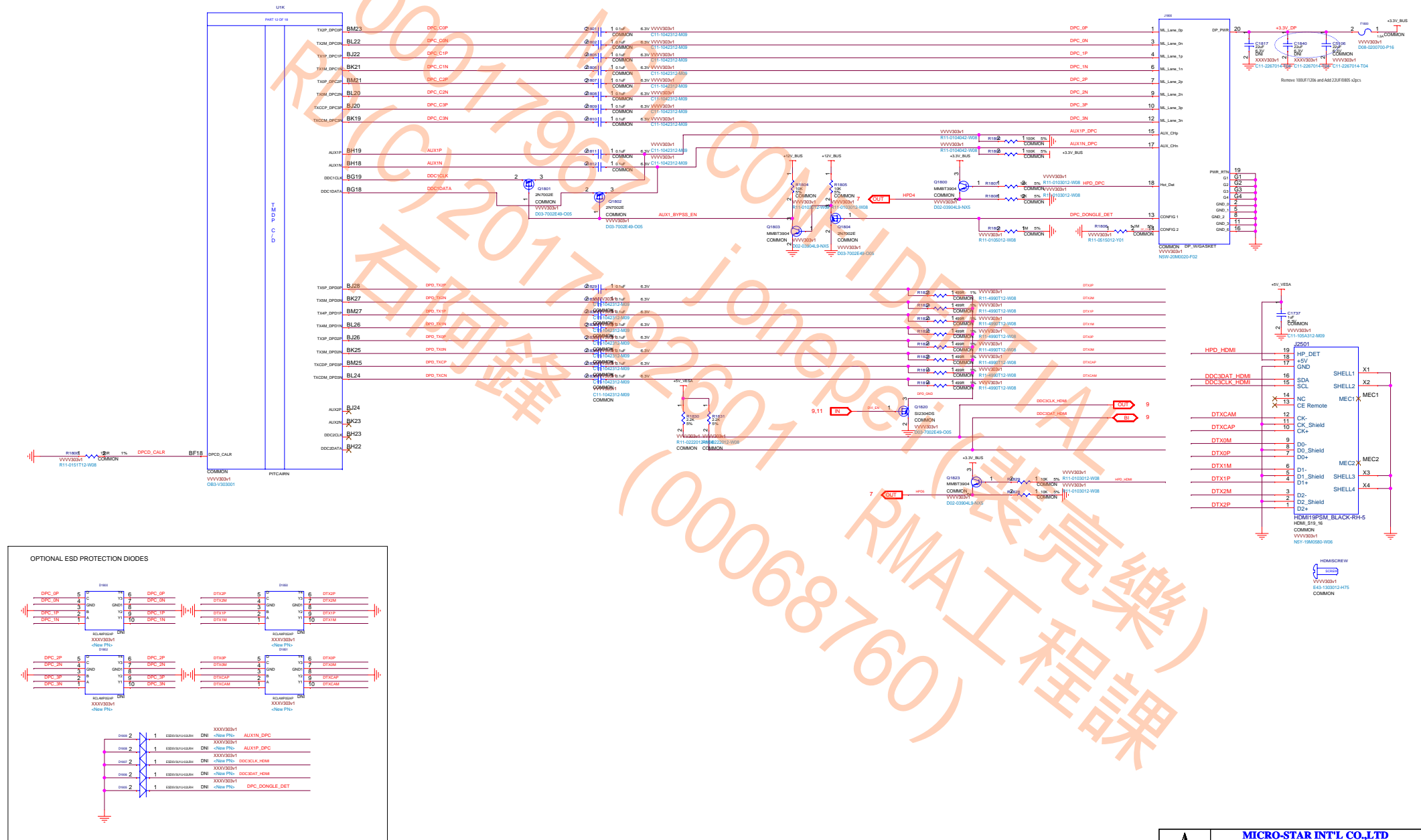


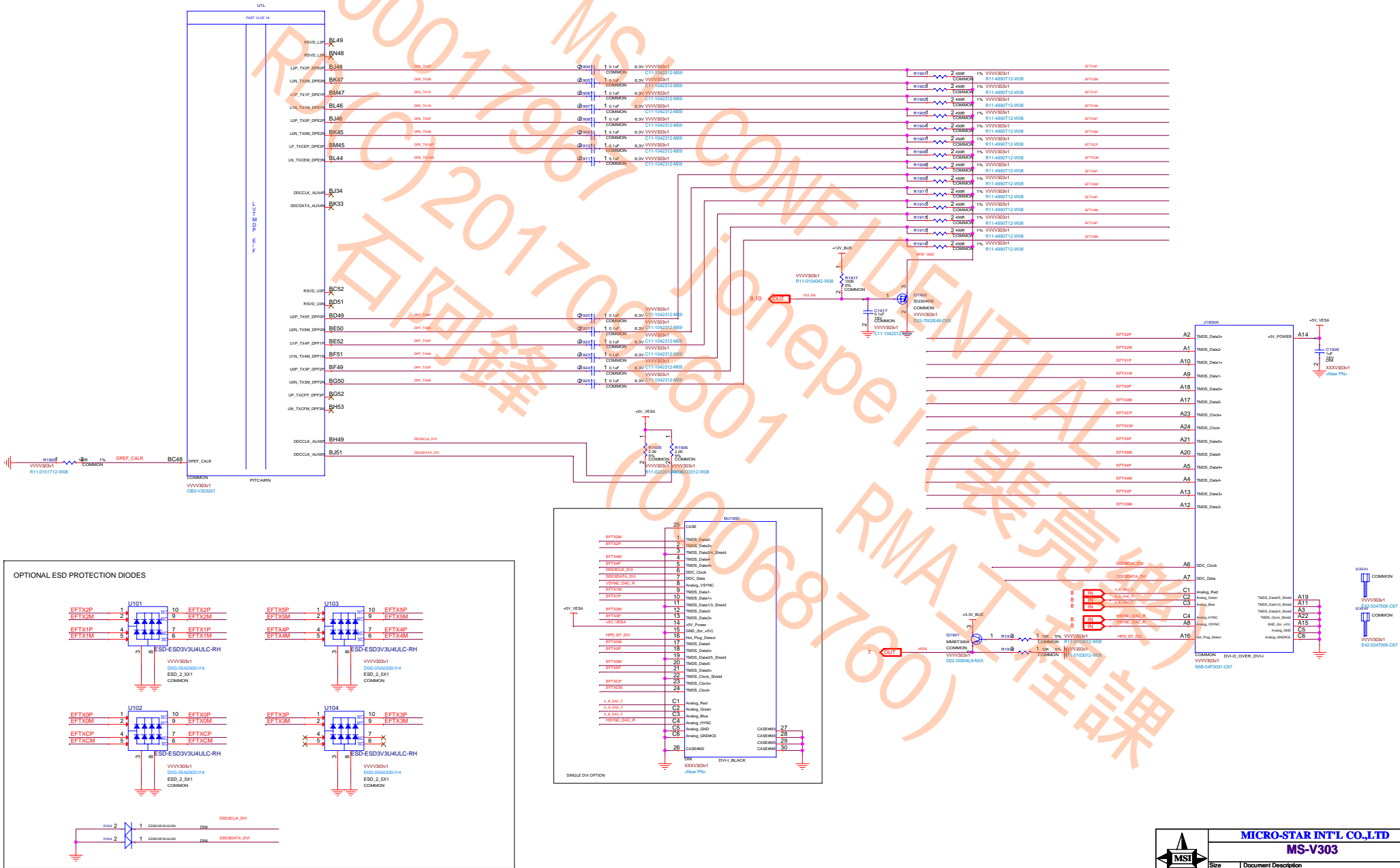
(1) PCI-EXPRESS EDGE CONNECTOR



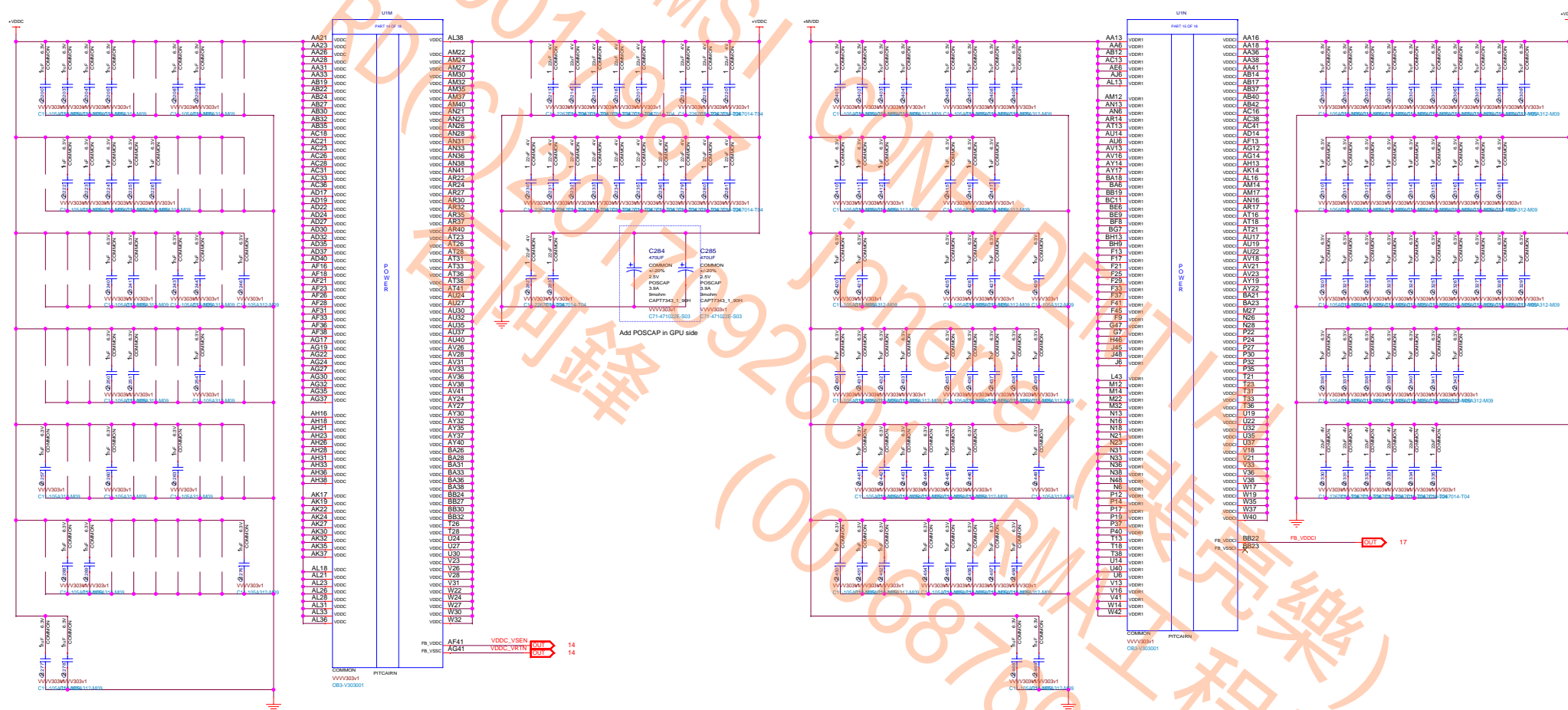
SYMBOL LEGEND	
DN1	DO NOT INSTALL
b or #	ACTIVE LOW
BUO	BRING UP ONLY
	DIGITAL GROUND
	ANALOG GROUND

(10) CURACAO TMDPCD DP HDMI





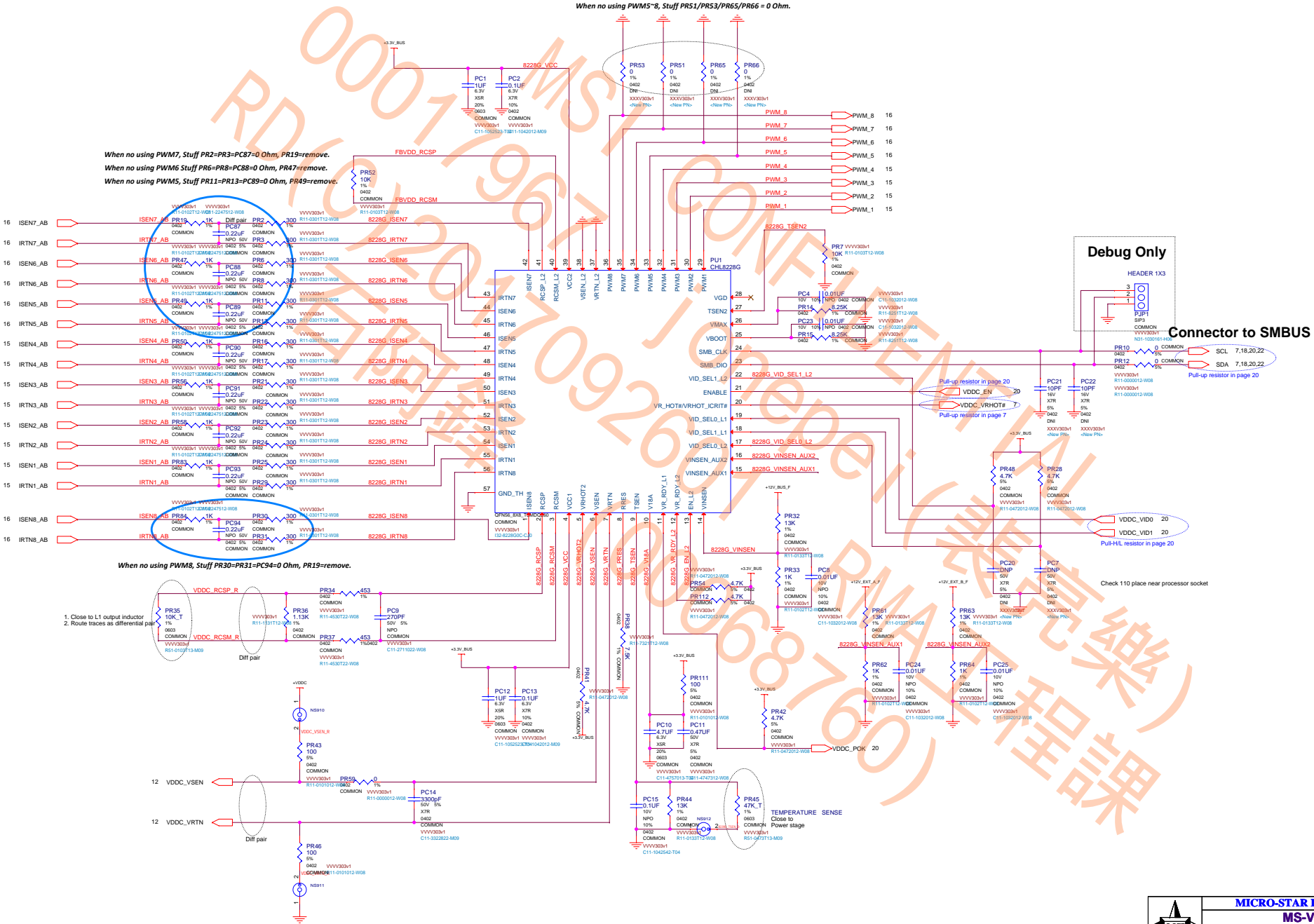
(12) CURACAO POWER

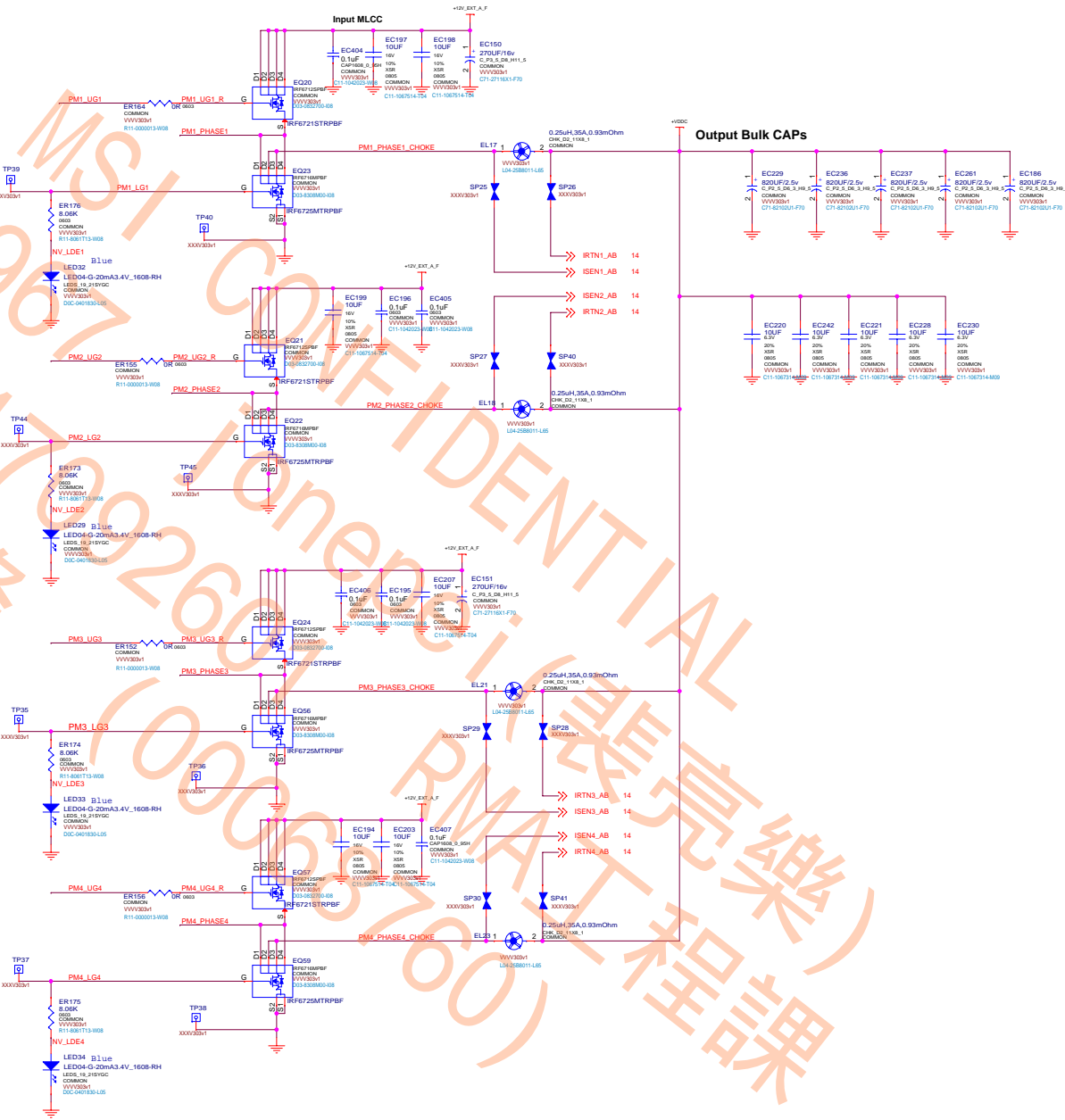
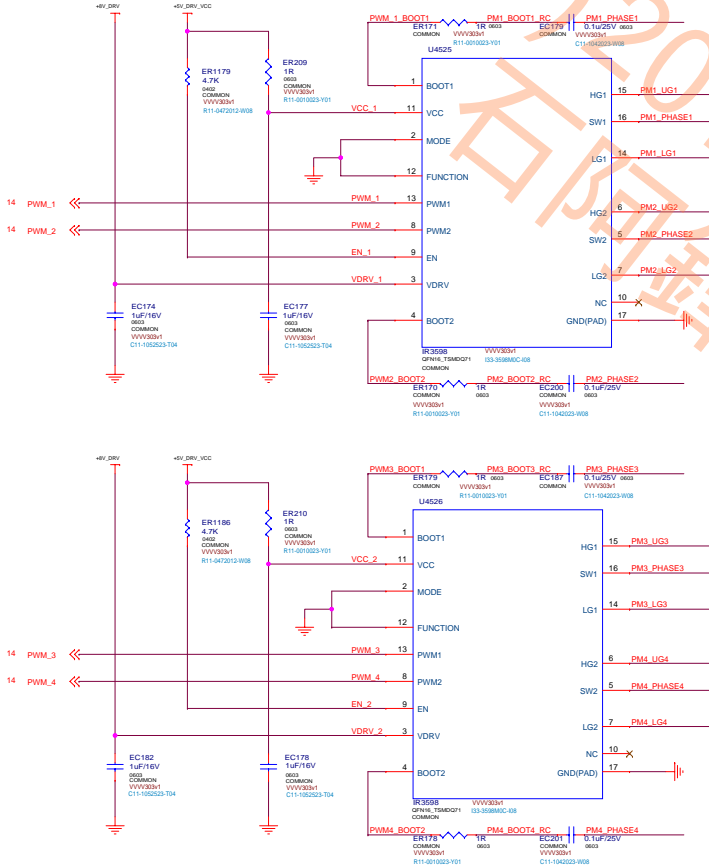
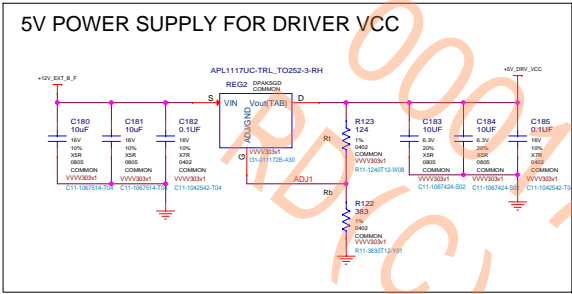


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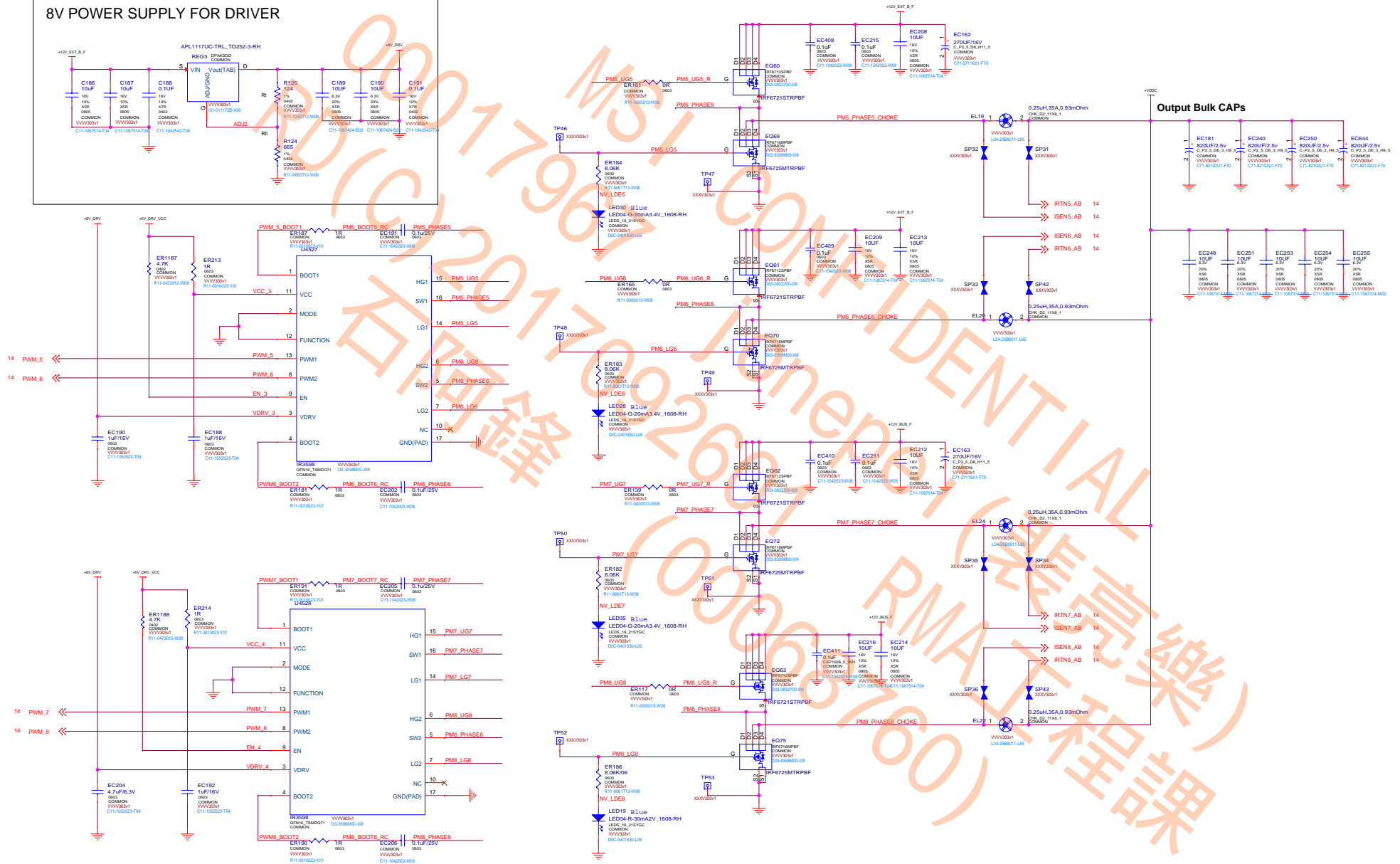
Size Custom	Document Description 12 CURAÇAO PITCAIRN POWER	Rev 1.0
Date: Thursday, August 01, 2013		Sheet 12 of 24

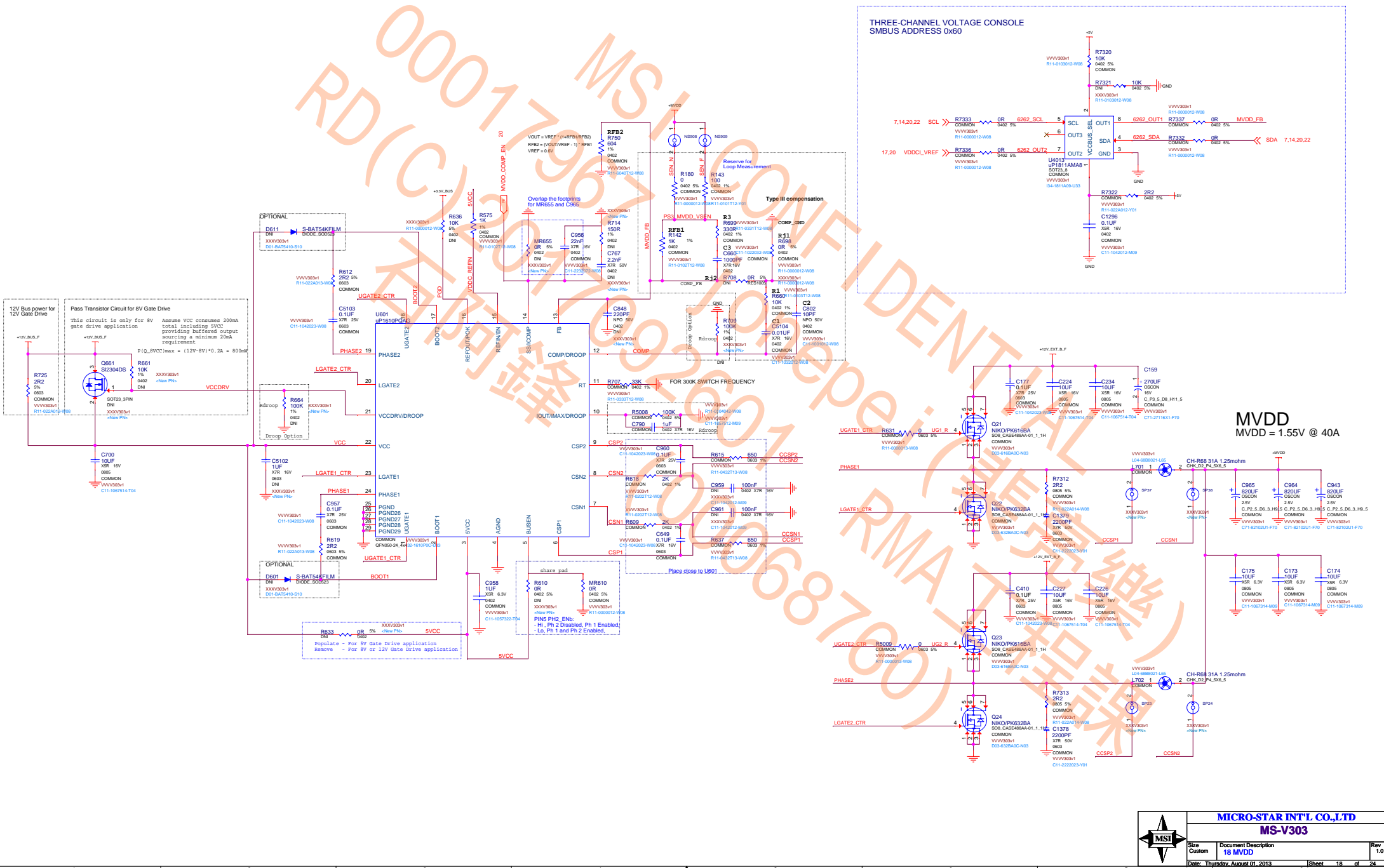




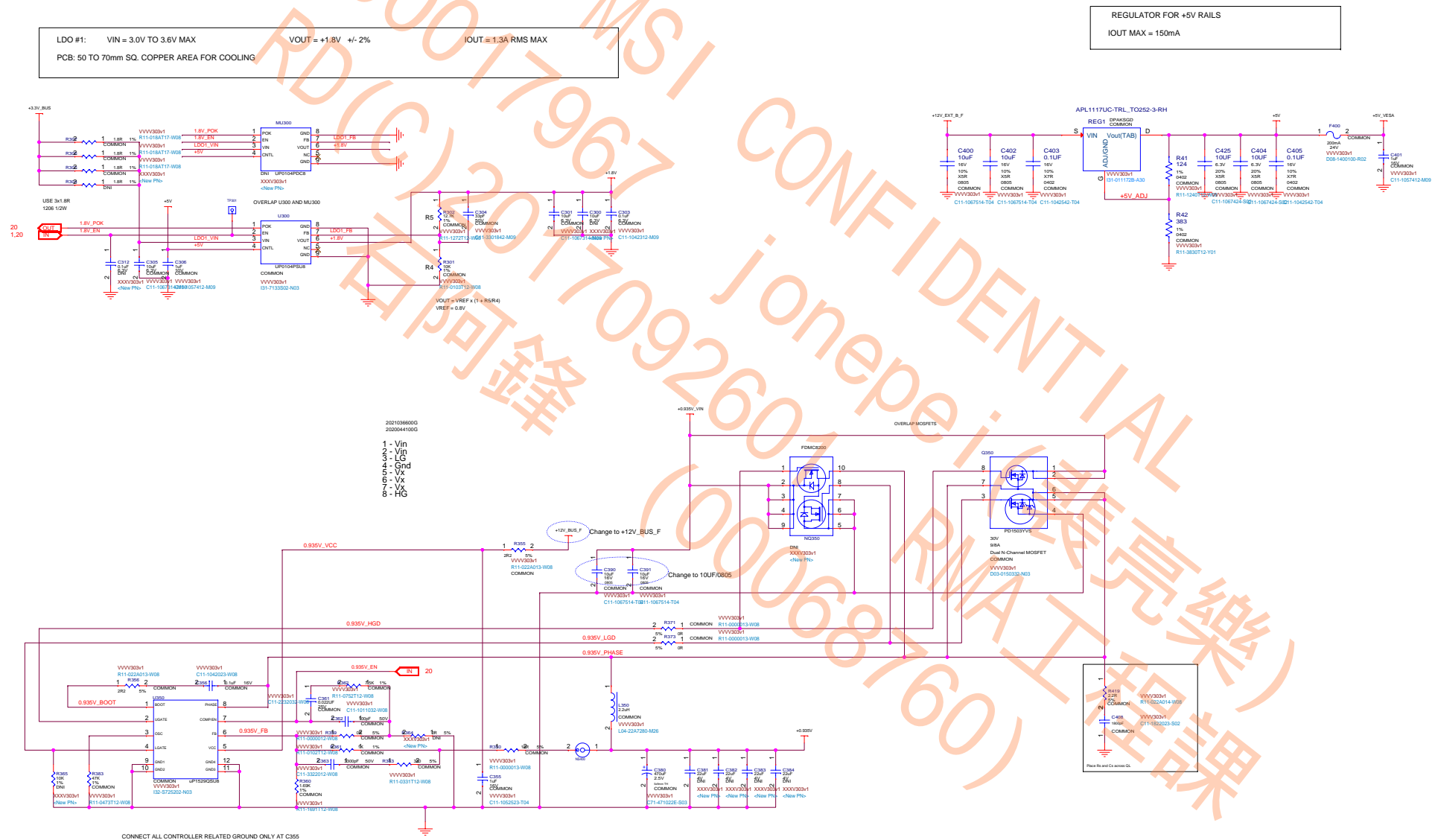


8V POWER SUPPLY FOR DRIVER

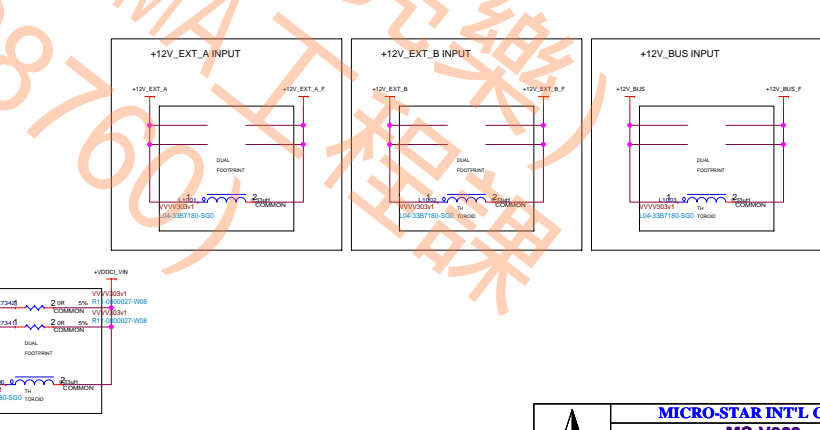
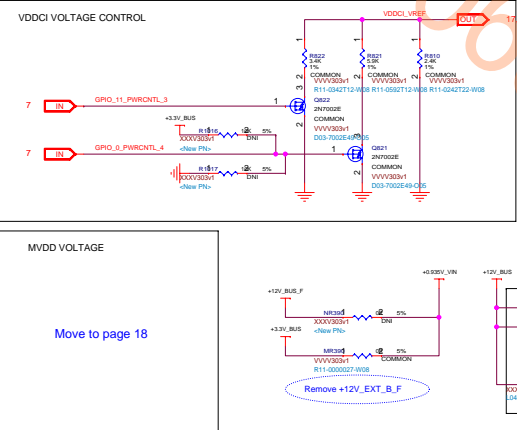
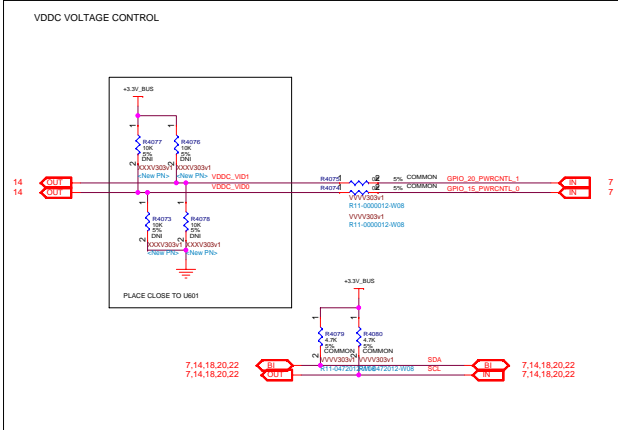
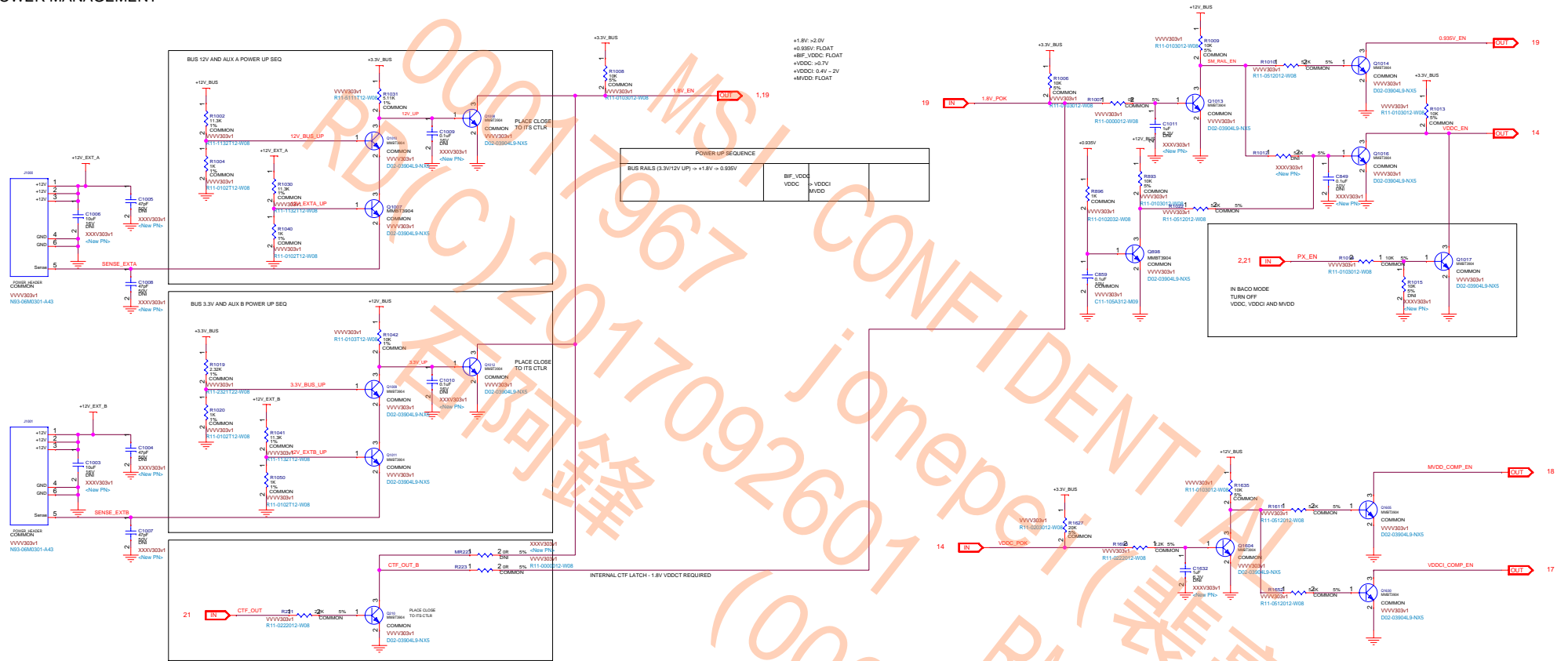


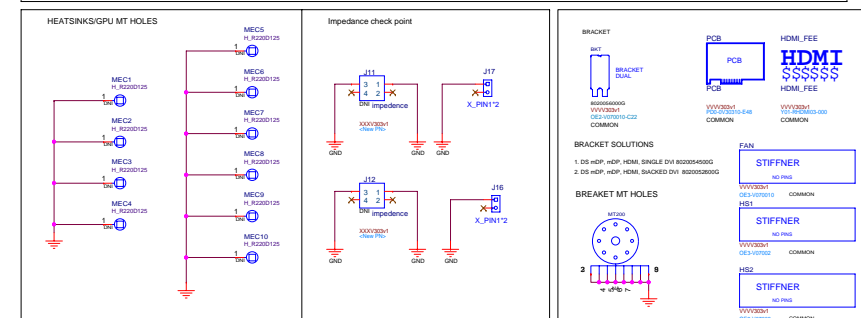
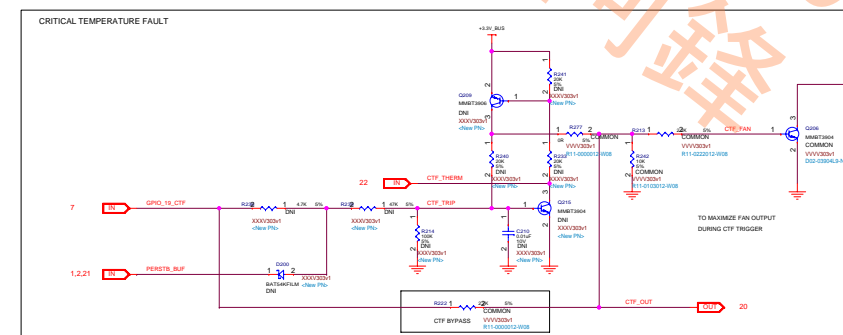


(18) SMALL RAIL REGULATOR

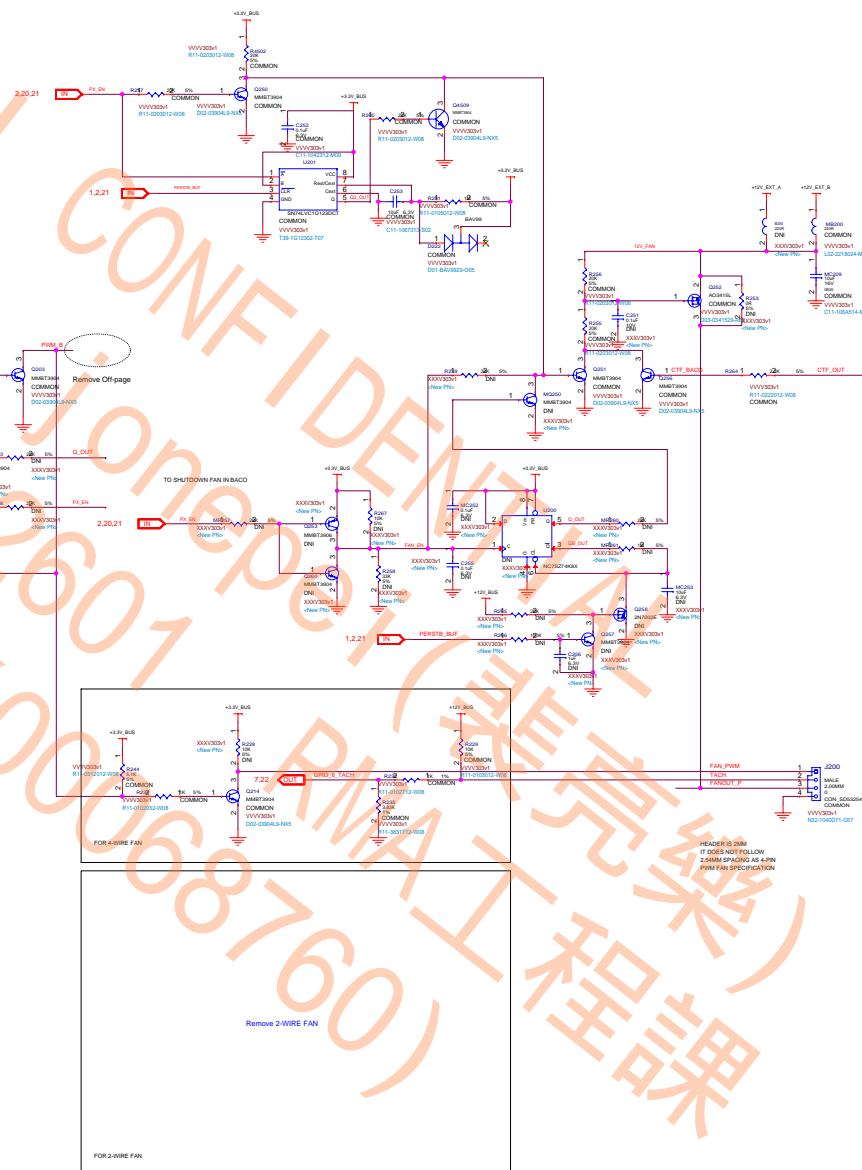


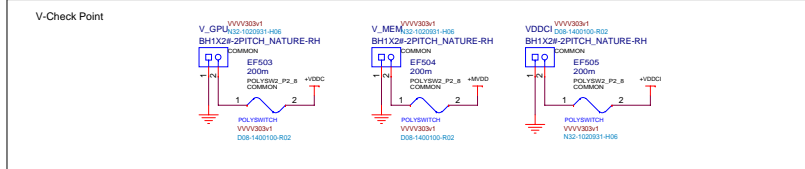
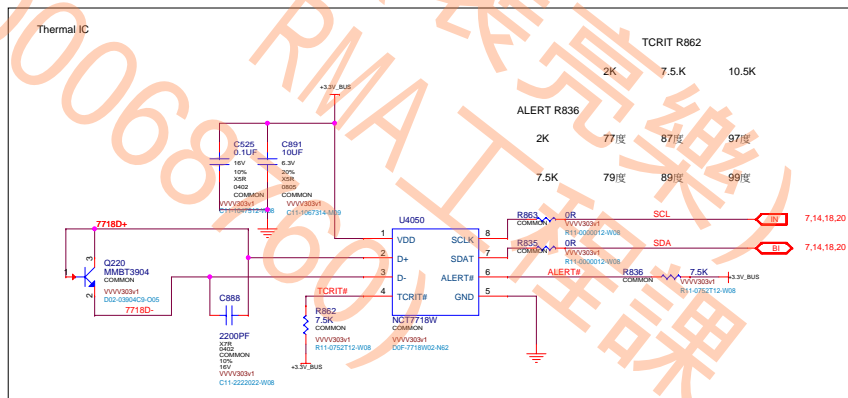
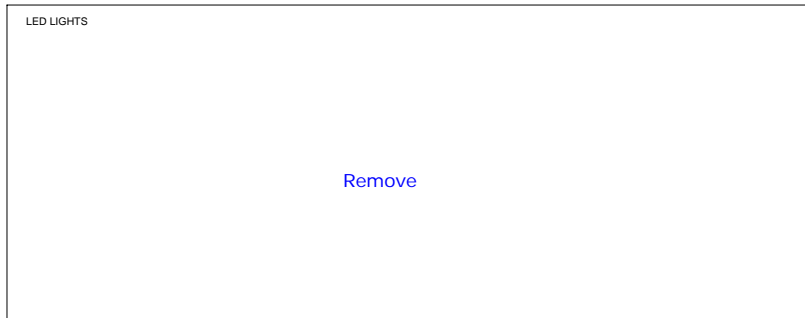
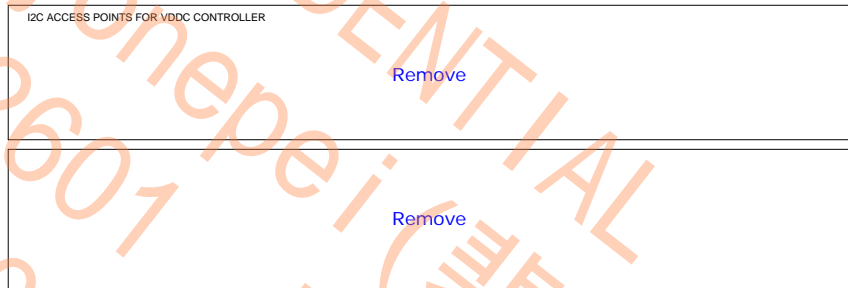
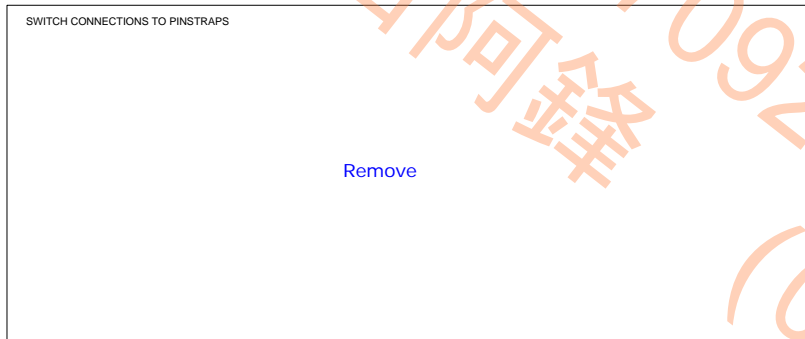
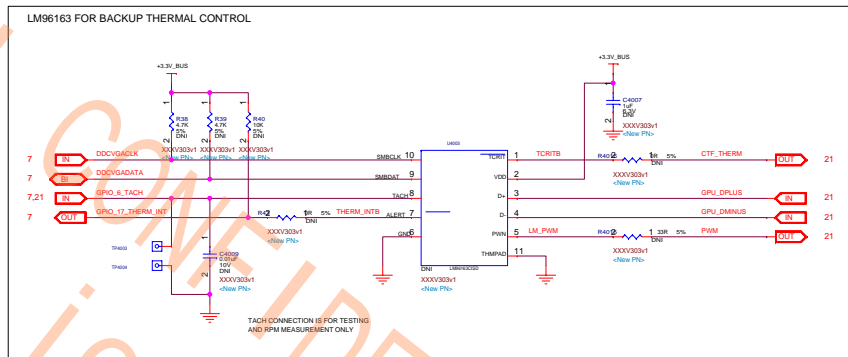
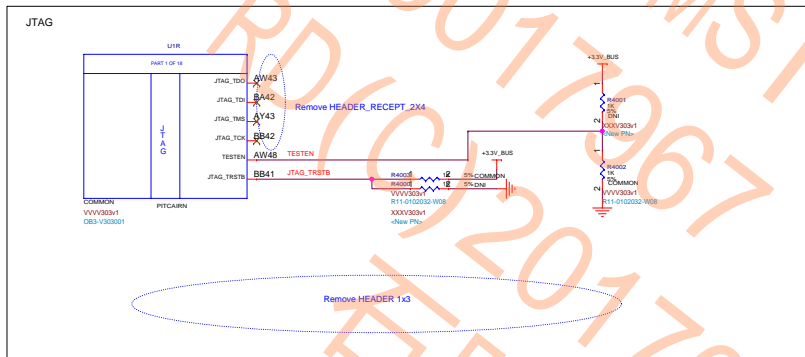
(19) POWER MANAGEMENT





The diagram illustrates a four-layer neural network structure. Each layer (FM1, FM2, FM3, FM4) consists of a cross-shaped node. The top-left arm of the cross is labeled 'DNE' and the bottom-right arm is labeled 'OPT'. The horizontal and vertical arms are labeled 'XXXX/32b/1' and 'APPLY'. The layers are connected in a sequence, with the 'OPT' output of one layer feeding into the 'DNE' input of the next layer.





0	00A	12/07/2012	INITIAL SCHEMATIC BASED ON C400
1	00B	30/10/2012	add R688,C98,C99
1	00C	25/12/2012	remove L1720 ~ L1733 remove NC pin for DP_VDDR/DP_VDDC
	00D	19/06/2013	update power sequence to make 0.95V power up before vddc
V303-1.0	01/08/2013	Page07 : Remove GPIO_14_HP2 off-page Add Dual-BIOS & Switch Page10 : Change J2501 footprint and Library Page11 : Add optional ESD Protection DIODES Page12 : Add C284/C285 (POSCAP) Remove some 1UF/0402 of VDDC Page14 : Change VDDC controller to 8228G Page15 : Add Driver IR3598 circuit Page16 : Add Driver IR3598 circuit Page17 : Change L801 footprint Change VDDCI_VIN Page18 : Page14 : Change MVDD controller to uP1610PQAG Page19 : Change +5V circuit Change 0.935V_VCC to +12V_BUS_F Page20 : Add R7341/R7342/L1506 Del R1090~R1095 Page21 : Remove 2-wire FAN circuit Page22 : Remove JTAG pin header Remove SWITCH CONNECTIONS TO PINSTRAPS Remove LED LIGHTS Remove I2C ACCESS POINTS FOR VDDC CONTROLLER Add V-Check Point and Thermal IC	